Description

LOW PASS FILTER

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of the filing date of Taiwan Application Ser. No. 092124750, filed Sep. 08, 2003, which is incorporated herein by reference. This application is a continuation-in-part of U.S. Application Ser. No. 10/707,803, filed Jan. 13, 2004, and U.S. Application Ser. No. 10/605,327, filed Sep. 23, 2003, both of which are incorporated herein by reference.

BACKGROUND OF INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a low pass filter, and more specifically, to a low pass filter with a large time constant.

[0004] 2. Description of the Prior Art

[0005] The low pass filter is a common device in various types of circuits including a conventional servo loop 10 shown in

Fig.1. Generally speaking, the conventional servo loop 10 is used for providing a high pass filtering characteristic between an input signal Vi and an output signal Vo. To act as a high pass filter, the servo loop 10 is composed of a gain device 12 and a low pass filter 14 connected in a negative feedback configuration. As shown in Fig.1, k/s represents a transfer function of the low pass filter 14, which includes a pole when s=0, while k is a constant corresponding to a time constant of the low pass filter 14.

[0006] Please refer to Fig.2 showing a circuit diagram of the low pass filter 14. Node A is connected to the output voltage Vo in Fig.1, and node B is fed back to the input voltage Vi in Fig.1. The low pass filter 14 is composed of an operational amplifier 16, a capacitor 18 (with capacitance C_1), and a resistor 20 (with resistance R_1) connected in an integrator configuration. In this configuration, the transfer function of the low pass filter 14 is as follows:

[0007]

$$\frac{k}{s} = -\frac{1}{sC_1R_1}$$

formula 1

[0008]

[0009] wherein C_1R_1 is the time constant of the low pass filter 14. Thus it can be seen by formula 1 that the constant k is inversely proportional to the time constant C_1R_1. That is, the larger the time constant is, the smaller k is. Therefore, for better high pass filtering characteristic of the servo loop 10, a larger time constant of the low pass filter 14 is preferable.

[0010] For a larger time constant, both the capacitor 18 and the resistor 20 of the low pass filter 14 need large values. However in an integrated circuit, a capacitor and a resistor having large values occupy too much area, so that the cost of the design increases accordingly.

SUMMARY OF INVENTION

[0011] It is therefore one of the many objectives of the present invention to provide a low pass filter with a large time constant.

[0012] According to embodiments of the present invention, a low pass filter is disclosed. The low pass filter includes a differential amplifier including a positive input end, a negative input end, a positive output end and a negative output end, a first resistive device coupled between the negative input end and a first node, a second resistive device coupled between the positive input end and the first node,

a third resistive device substantially the same as the second resistive device coupled between the negative input end and a second node, a fourth resistive device substantially the same as the first resistive device coupled between the positive input end and the second node, a first capacitive device coupled between the negative input end and the positive output end, and a second capacitive device substantially the same as the first capacitive device coupled between the positive input end and the negative output end.

[0013] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the embodiments that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0014] Fig.1 illustrates a conventional servo loop.

[0015] Fig.2 is a circuit diagram of a conventional low pass filter.

[0016] Fig.3 illustrates a low pass filter according to an embodiment of the present invention.

[0017] Fig.4 illustrates an adjustable impedance circuit according to an embodiment of the present invention.

[0018] Fig.5 illustrates an adjustable impedance circuit according to an embodiment of the present invention.

[0019] Fig.6 is a timing diagram of the first control signal and the second control signal.

[0020] Fig.7 illustrates a low pass filter according to another embodiment of the present invention.

DETAILED DESCRIPTION

[0021] Please refer to Fig.3 showing a low pass filter according to an embodiment of the present invention. In this embodiment, the low pass filter 30 is connected in a differential configuration, for low pass filtering a first input signal Vi^+ and a second input signal Vi^-, in order to generate a first output signal Vo^+ and a second output signal Vo^-.

[0022] The low pass filter 30 in Fig.3 includes a differential amplifier 32 having a positive input end C, a negative input end D, a positive output end E, and a negative output end F. A first resistive device 34 is coupled between the negative input end D and a first node G, a second resistive device 36 is coupled between the positive input end C and the first node G.A third resistive device 38 being substantially the same as the second resistive device 36 is coupled between the negative input end D and a second node H, and a fourth resistive device 40 being substantially the

same as the first resistive device 34 is coupled between the positive input end C and the second node H. A first capacitive device 42 is coupled between the negative input end D and the positive output end E, and a second capacitive device 44 being substantially the same as the first capacitive device 42 is coupled between the positive input end C and the negative output end F. The first node G receives the first input signal Vi^+, and the second node H receives the second input signal Vi^-. The positive output end E is for outputting the first output signal Vo^+, and the negative output end F is for outputting the second output signal Vo^-.

[0023] In order to make the low pass filter 30 have a large time constant, the resistance of the first resistive device 34 and the fourth resistive device 40 is set to be R_1, and the resistance of the second resistive device 36 and the third resistive device 38 is set to be $R_1(1+\alpha)$, wherein $|\alpha|<<1$. That is, the value of the first resistive device 34 is very close to the value of the second resistive device 36, and the value of the third resistive device 38 is very close to the value of the fourth resistive device 40. In this case, the relative equation of current at the negative input end of the differential amplifier 32 is shown as follows:

[0024]

$$\frac{V_o}{V_i} = \frac{\alpha}{sC_1R_1(1+\alpha)} \cong \frac{\alpha}{sC_1R_1}$$

formula 2

[0025]

[0026] From formula 2, the time constant of the low pass filter 30 is equivalent to (C_1R_1/α), and since the absolute value of α is far less than 1, in the configuration of the low pass filter 30, even if the resistance R_1 is not a large value, the time constant can be a very large value. In such a manner, the low pass filter 30 according to this embodiment of the present invention does not require a resistive device occupying a large area for a large time constant. Please notice that, the relative equation of current at the positive input end of the differential amplifier 32 is the same to the relative equation of current at the negative input end of the differential amplifier 32 mentioned above, thus a further description is hereby omitted.

[0027] In order to manufacture two resistive devices with very close values, such as R_1 and $R_1(1+\alpha)$ having an α value complying with the requirement, the present invention discloses two embodiments of an adjustable impedance

circuit to implement the impedance of R_1 and $R_1(1+\alpha)$.

[0028] Please refer to Fig.4 showing an adjustable impedance circuit 100 according to an embodiment of the present invention. In this embodiment, a first impedance 102 is a resistor with resistance R_2, a second impedance 106 is a resistor with resistance R_3, a first switch device 104 includes a first switch 110 for switching on and off according to a first control signal $CTRL_1$, and a second switch device 108 includes a third switch 112 for switching on and off according to a second control signal $CTRL_2$. In this embodiment, the first switch 110 and the third switch 112 are transmission gates composed of an NMOS transistor and a PMOS transistor. The gates of the NMOS transistor and the PMOS transistor control the switching of the transmission gate according to a control signal and an inverted control signal respectively.

[0029] Please refer to Fig.5 showing an adjustable impedance circuit 100 according to another embodiment of the present invention. In this embodiment, a first switch device 104 includes a first switch 114 and a second switch 118 electrically connected in series with a first impedance 102 at either end, for switching on and off according to a first control signal $CTRL_1$. Similarly, a second switch de-

vice 48 includes a third switch 116 and a fourth switch 120 electrically connected in series with a second impedance 106 at either end, for switching on and off according to a second control signal $CTRL_2$.

[0030] In this embodiment, the first switch 114 and the second switch 118 are MOS transistors switching on and off according to the first control signal $CTRL_1$, and the third switch 116 and the fourth switch 120 are also MOS transistors switching on and off according to the second control signal $CTRL_2$.

[0031] Please refer to Fig.6 showing a timing diagram of an example of the first control signal $CTRL_1$ and the second control signal $CTRL_2$. In Fig.6, both the first control signal $CTRL_1$ and the second control signal $CTRL_2$ are periodic signals having a period of Ttotal. The time duration of the first control signal $CTRL_1$ at a high level (i.e., the time duration of the second control signal $CTRL_2$ at a low level) is T_1, and the time duration of the second control signal $CTRL_2$ at a high level (i.e., the time duration of the first control signal $CTRL_1$ at a low level) is T_2. In this embodiment, the first control signal $CTRL_1$ and the second control signal $CTRL_2$ are complementary to each other, but the present invention is not limited thereto.

[0032] As shown in Fig.6, when the first control signal $CTRL_1$ is at a high level and the second control signal $CTRL_2$ is at a low level, the first switch device 104 is turned on so that the first impedance 102 is electrically connected between the third node I and the fourth node J. In the mean time, the second switch device 108 is turned off so that the second impedance 106 is disconnected from the third node I and the fourth node J. Therefore between time t_0 and time t_1, the impedance of the adjustable impedance circuit 100 between the third node J and the fourth node J is equivalent to impedance R_2. On the contrary, when the first control signal $CTRL_1$ is at a low level and the second control signal $CTRL_2$ is at a high level, the first switch device 104 is turned off so that the first impedance 102 is disconnected from the third node I and the fourth node J. In the mean time, the second switch device 108 is turned on so that the second impedance 106 is electrically connected between the third node I and the fourth node J. Therefore between time t_1 and time t_2, the impedance of the adjustable impedance circuit 100 between the third node I and the fourth node J is equivalent to impedance R_3.

[0033] According to aforementioned, by periodically switching

the first control signal $CTRL_1$ and the second control signal $CTRL_2$, the equivalent impedance Zeq between the third node I and the fourth node J can be shown as follows:

[0034]

$$Zeq = \frac{T_1 R_2 + T_2 R_3}{T_{total}} = DC_1 R_2 + DC_2 R_3$$

formula 3

[0035] wherein DC_1 is the duty cycle of $CTRL_1$, and DC_2 is the duty cycle of $CTRL_2$. Since the behavior of a digital signal (e.g. the duty cycle of the first and the second control signal) can be accurately controlled under present technology, by controlling the adjustable impedance circuit 100 with the first control signal $CTRL_1$ and the second control signal $CTRL_2$, two impedances with very close values can be obtained.

[0036] Please refer to Fig.7 showing a low pass filter according to another embodiment of the present invention. In addition to the low pass filter 30 in Fig.3, the low pass filter 80 in Fig.7 has at its input end a fifth resistive device 84 coupled between a first node G and a first input signal Vi^+. A sixth resistive device 86 substantially the same as the fifth resistive device 84 is coupled between a second node H

and a second input signal Vi^-, and a seventh resistive device 82 is coupled between the first node G and the second node H. Assuming that the resistance of the seventh resistive device 82 is $2R_2$, and the resistances of the fifth resistive device 84 and the sixth resistive device 86 are R_3, in the configuration shown in Fig.9, the equation of the low pass filter 80 is shown as follows:

[0037]

$$\frac{Vo}{Vi} \cong \frac{\alpha}{sC_1 R_1} \times \frac{R_2}{R_2 + R_3}$$

formula 4

[0038] As shown in formula 4, the time constant of the low pass filter 80 is equivalent to $(C_1 R_1 / \alpha) \times ($

$$\frac{R_2 + R_3}{R_2}$$

), and since the absolute value of α is far less than 1, and (

$$\frac{R_2 + R_3}{R_2}$$

) is larger than 1, in the configuration of the low pass filter 80, even if the resistance R_1 is not a large value, the time constant can still be a very large value. As described above, the low pass filter 80 not only obtains a large time constant using the first resistive device 34, the second resistive device 36, the third resistive device 38, and the fourth resistive device 40, but also increases the time constant using the fifth resistive device 84, the sixth resistive device 86, and the seventh resistive device 82.

[0039] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.